IN THE CLAIMS

A listing of all claims and their current status in accordance with 37 C.F.R. § 1.121(c) is provided below.

1-18. (Cancelled)

19. (Currently amended) A semiconductor device substantially impervious to the effects of buckling, said device comprising:

a) a single first planarization layer ~~superjacent~~ disposed on a semiconductor substrate, the single first planarization layer having a first reflow temperature and a first thermal coefficient of expansion;

b) a barrier film ~~superjacent said substrate, said barrier film having a structural integrity~~disposed on the single first planarization layer; and

c) a single second planarization layer ~~superjacent said~~disposed on the barrier film, ~~said second layer being isolated froms aid first layer by said barrier film when a temperature of at least approximately 700°C is applied~~the single second planarization layer having a second reflow temperature and a second thermal coefficient of expansion, wherein the barrier film does not reflow at the first or second reflow temperatures and retains its structural integrity to isolate the single first planarization layer from the single second planarization layer, thereby preventing ~~said~~ the single first planarization layer and ~~said~~ the single second planarization layer ~~fron~~ from interacting, and enabling ~~said~~ the single first planarization layer and ~~said~~ the single second planarization layer to uniformly reflow.

20. (Currently amended) A semiconductor device substantially impervious to the effects of buckling, according to ~~Claim~~ claim 19, wherein said barrier film comprises at least ~~one~~ one of titanium nitride, tantalum nitride, titanium oxide, tantalum oxide, silicon dioxide, silicon nitride and tetraethylorthosilicate ("TEOS").

21. (Currently amended) A semiconductor device substantially impervious to the effects of buckling, according to claim 19, wherein ~~said~~ the single first planarization layer comprises at least one of tungsten, titanium, tantalum, copper, aluminum, single crystal silicon, polycrystalline silicon, amorphous silicon, borophosphosilicate glass ("BPSG") and tetraethylorthosilicate ("TEOS").

22. (Currently amended) A semiconductor device substantially impervious to the effects of buckling, according to claim 19, wherein said single second planarization layer comprises at least one of tungsten, titanium, tantalum, copper, aluminum, single crystal silicon, polycrystalline silicon, amorphous silicon, borophosphosilicate glass ("BPSG") and tetraethylorthosilicate ("TEOS").

23. (Currently amended) A semiconductor device substantially impervious to the effects of buckling, according to claim 19, wherein ~~said~~ the single second planarization layer comprises a metal.

24. (Currently amended) A semiconductor device substantially impervious to the effects of buckling, according to claim 19, wherein ~~said~~ the single second planarization layer comprises a refractive metal.

25. (Currently amended) A semiconductor device substantially impervious to the effects of buckling, according to claim 19, wherein ~~said~~ the single second planarization layer comprises at least one of boroposphosilicate glass ("BPGS") and tetraethylorthosilicate ("TEOS").

26. (Currently amended) A planar multilayered semiconductor device comprising:

a substrate;

a first single flowable layer disposed on the substrate and having a thermal coefficient of expansion;

a nitride film ~~superjacent said~~disposed on the first layer; and

~~another~~ a second single flowable layer ~~superjacent said~~disposed on the nitride film, ~~said another~~the second single flowable layer having another thermal coefficient of expansion, wherein the nitride film retains its structural integrity at the reflow temperatures of the first single flowable layer and the second single flowable layer, thereby preventing the first single flowable layer and the second single flowable layer from interacting, and enabling the first single flowable layer and the second single flowable layer to uniformly reflow.

27. (Currently amended) The planar multilayered semiconductor device according to claim 26, wherein said nitride film isolates ~~said~~ the first single flowable layer from ~~said another~~the

second single flowable layer, thereby preventing ~~said~~ the first single flowable layer and ~~said another~~the second single flowable layer from interacting when heated.

28. (Currently amended) The planar multilayered semiconductor device according to claim 27, wherein ~~said~~ the first single flowable layer and ~~said another~~the second single flowable layer reflow at a temperature of at least 700°C.

29. (Previously presented) The planar multilayered semiconductor device according to claim 28, wherein said nitride film comprises at least one of titanium nitride, tantalum nitride, and silicon nitride.

30. (Currently amended) The planar multilayered semiconductor device according to claim 29, wherein ~~said~~ the first single flowable layer comprises at least one of tungsten, titanium, tantalum, copper, aluminum, single crystal silicon, polycrystalline silicon, amorphous silicon, borophosphosilicate glass ("BPSG") and tetraethylorthosilicate ("TEOS").

31. (Currently amended) The planar multilayered semiconductor device according to claim 30, wherein ~~said~~ the ~~first~~second single flowable layer comprises at least one of tungsten, titanium, tantalum, copper, aluminum, borophosphosilicate glass ("BPSG") and tetraethylorthosilicate ("TEOS").

32. (Currently amended) The planar multilayered semiconductor device according to claim 30, wherein ~~said~~ the first single flowable layer comprises at least one of single crystal silicon, polycrystalline silicon, amorphous silicon.

33. (Currently amended) A multilayer heterostructure semiconductor device having a planar configuration comprising:

a semiconductor substrate;

a first single planarization layer disposed ~~superjacent said~~on the substrate, ~~said~~ the single first planarization layer having a first thermal coefficient of expansion and a first reflow temperature;

a barrier film disposed ~~superjacent said~~on the single planarization layer, said barrier film having structural integrity; and

~~another~~ a single second layer disposed ~~superjacent said~~on the barrier film, ~~said~~ wherein the barrier film ~~for preventing~~prevents ~~said~~ the single first planarization layer and ~~said another~~the single second layer from interacting when ~~heated~~the single first planarization layer is heated to a temperature above the first reflow temperature, ~~said~~ the ~~another~~ single second layer having a second thermal coefficient of expansion.

34. (Previously presented) The multilayered heterostructure semiconductor device according to claim 33, wherein said barrier film comprises at least one of titanium nitride, tantalum nitride, titanium oxide, silicon nitride, tantalum oxide, silicon dioxide, borophosphosilicate glass ("BPSG") and tetraethylorthosilicate ("TEOS").

35. (Currently amended) The multilayered heterostructure semiconductor device according to claim 34, wherein said single first planarization layer comprises at least one of tungsten, titanium, tantalum, copper, aluminum, single crystal silicon, polycrystalline silicon, amorphous silicon, borophosphosilicate glass ("BPSG") and tetraethylorthosilicate ("TEOS").

36. (Currently amended) The multilayered heterostructure semiconductor device according to claim 35, wherein ~~said another~~the single second layer comprises at least one of tungsten, titanium, tantalum, copper, aluminum, borophosphosilicate glass ("BPSG") and tetraethylorthosilicate ("TEOS").

37. (Currently amended) The multilayered heterostructure semiconductor device according to claim 33, wherein ~~said~~ the single first planarization layer and ~~said another~~the single second layer reflow at a temperature of at least 700°C.

38. (Previously presented) The multilayered heterostructure semiconductor device according to claim 37, wherein said structural integrity of said barrier layer is maintained when heated to a temperature of at least 700°C.

39. (New) An apparatus, comprising:

a first layer at a temperature of at least 700°C, the first layer being in a reflow state;

a second layer at the temperature of at least 700°C, the second layer being in a reflow state;

a barrier layer at a temperature of at least 700°C, the barrier layer being disposed between the first and second layers, wherein the barrier layer is not in a reflow state and maintains its structural integrity to isolate the first layer from the second layer.

40. (New) The apparatus of claim 39, wherein the first layer comprises at least one of tungsten, titanium, tantalum, copper, aluminum, borophosphosilicate glass ("BPSG") and tetraethylorthosilicate ("TEOS").

41. (New) The apparatus of claim 39, wherein the second layer comprises at least one of tungsten, titanium, tantalum, copper, aluminum, borophosphosilicate glass ("BPSG") and tetraethylorthosilicate ("TEOS").

42. (New) The apparatus of claim 39, wherein the barrier layer comprises at least one of titanium nitride, tantalum nitride, titanium oxide, silicon nitride, tantalum oxide, silicon dioxide, borophosphosilicate glass ("BPSG") and tetraethylorthosilicate ("TEOS").